UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/711,677	09/30/2004	Han-Tung Hsu	13130-US-PA	5676

31561 7590 04/06/2006

JIANQ CHYUN INTELLECTUAL PROPERTY OFFICE
7 FLOOR-1, NO. 100
ROOSEVELT ROAD, SECTION 2
TAIPEI, 100
TAIWAN

EXAMINER	
CHIU, TSZ K	
ART UNIT	**PAPER NUMBER**
2822	

DATE MAILED: 04/06/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/711,677	HSU ET AL.	
	Examiner	Art Unit	
	Tsz K. Chiu	2822	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *30 September 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) *15-20* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-14* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Applicant's Election

Applicant's election without traverse of group I, claims 1-14, in the reply filed on February 20, 2006 is acknowledged.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-2 and 6-7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chu et al. (20050062910) in view of Hsu et al. (6,975,377).

With respect to claim 1-2, Chu disclose a transparent substrate (300, for example fig. 5A); a thin film transistor array (paragraph 6, lines 1-3), disposed over the transparent substrate within the pixel region (214, for example fig. 2), wherein the thin film transistor array at least comprises a first conductive layer (302 or 306, for example fig. 2) and a second conductive layer (306 or 302, for example fig. 2); a plurality of first lead lines (218, for example fig. 2), disposed over the transparent substrate within the peripheral region (216, for example fig. 2), wherein both the first lead lines and the first conductive layer belong to a same film layer; a plurality of second lead lines (222, for example fig. 3), disposed over the transparent substrate within the peripheral region

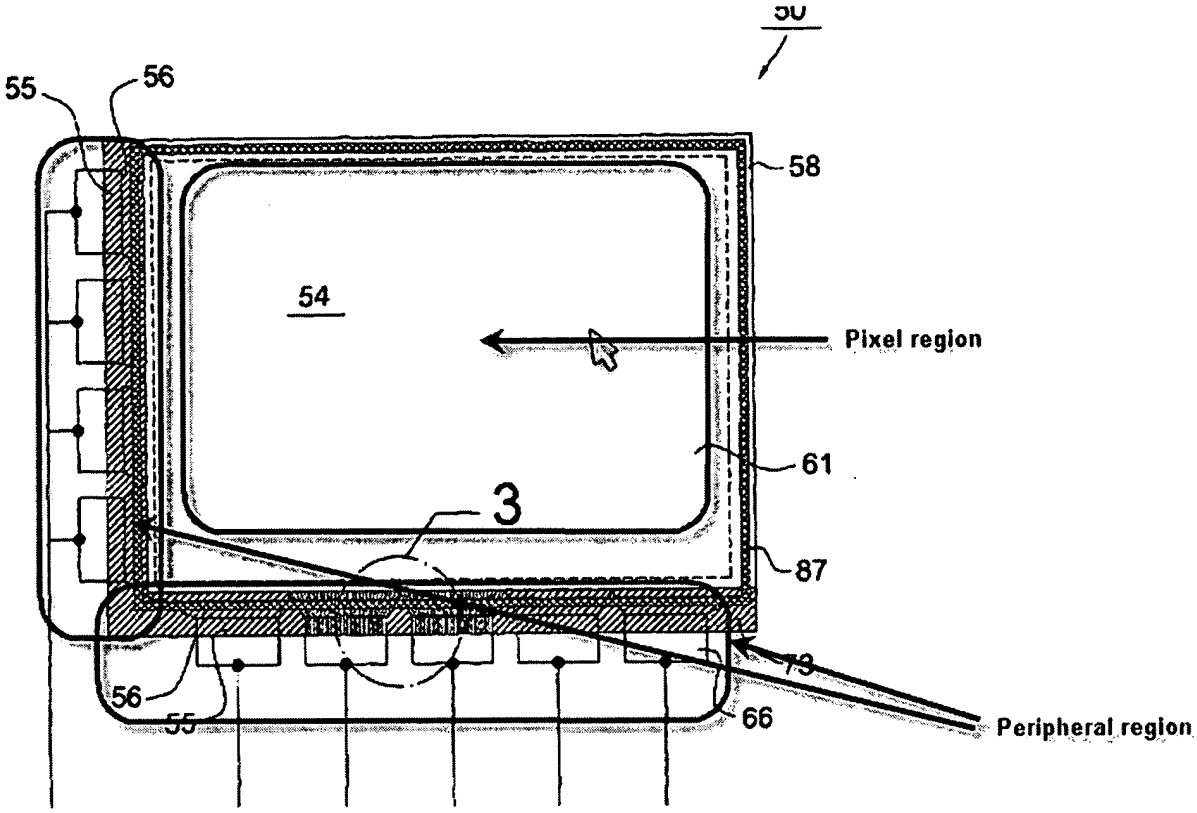
(216, for example fig. 3), wherein both the second lead lines and the second conductive layer belong to a same film layer.

However, Chu did not disclose a first shielding layer, disposed. over the transparent substrate within the peripheral region to cover the gaps between neighboring first lead lines, and both the first shielding layer and the second conductive layer belong to a same film layer.

Hsu discloses a first shielding layer (77, for example fig. 8), disposed over the transparent substrate (column 3, lines 1-2) within the peripheral region (see drawing below) to cover the gaps between neighboring first lead lines (67, for example fig. 8), and both the first shielding layer and the second conductive layer belong to a same film layer; Hsu also discloses a second shielding layer (left side of 56, for example fig. 2) disposed over the transparent substrate (column 3, lines 1-2) within the peripheral region (see drawing below) to cover the gaps between neighboring second lead lines (67, for example fig. 8), and both the second shielding layer and the first conductive layer belong to the same film layer.

Since Chu and Hsu are both from the same field of endeavor LCD device, the purpose disclosed by Hsu would have been recognized in the pertinent art of Chu.

Therefore, it would have been obvious to one having ordinary skill in the art at the time of the invention to have Hsu the light cover shield use in Chu's invention for the purpose of prevent light leakage (column1, lines 8-11).



With respect to claim 6, Chu discloses wherein the first conductive layer comprises a gate layer (302, for example fig. 3), and the second conductive layer comprises a source/drain layer (306, for example fig. 3).

With respect to claim 7, Chu discloses wherein the first conductive layer comprises a source/drain layer (306, for example fig. 3), and the second conductive layer comprises a gate layer (302, for example fig. 3).

Claims 3-5 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chu et al. (20050062910) and Hsu as applied to claim 1, above and further in view of Sekine (6,580,486),

With respect to claim 3-5, Chu discloses invention set forth to claim 1-3, but did not disclose a common voltage is applied to the first shielding layer, second shielding layer.

Sekine discloses wherein a common voltage is applied to the first shielding layer, second shielding layer

Since Chu and Sekine are both from the same field of endeavor LCD device, the purpose disclosed by Sekine would have been recognized in the pertinent art of Chu.

Therefore, it would have been obvious to one having ordinary skill in the art at the time of the invention to have Sekine common voltage use in Chu's invention f or the purpose of reduce noise generated following voltage fluctuation between the data lines, and to improve image quality.

Claims 8-9 and 13-14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chu et al. (20050062910) in view of Hsu et al. (6,975,377).

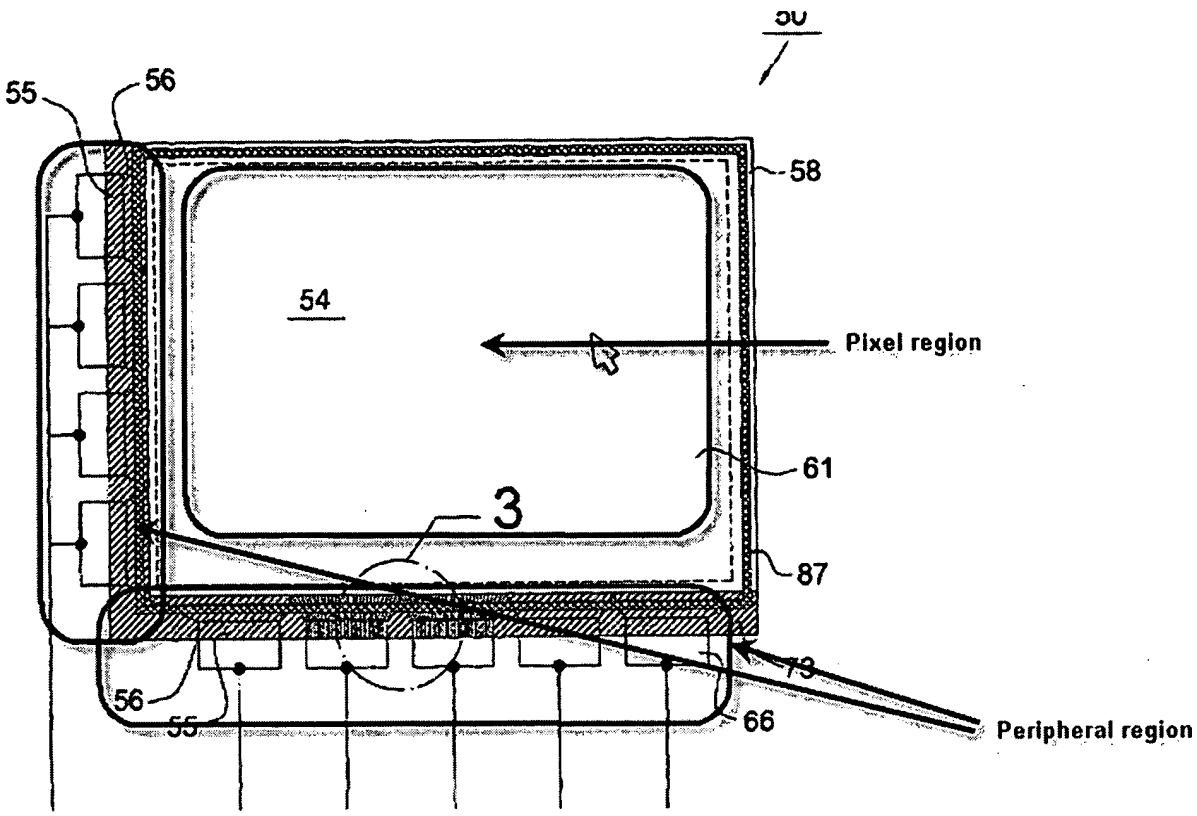
With respect to claim 8-9 and 13-14, Chu disclose a transparent substrate (300, for example fig. 5A); a thin film transistor array (paragraph 6, lines 1-3), disposed over the transparent substrate within the pixel region (214, for example fig. 2), wherein the thin film transistor array at least comprises a first conductive layer (302 or 306, for example fig. 2) and a second conductive layer (306 or 302, for example fig. 2); a plurality of first lead lines (218, for example fig. 2), disposed over the transparent substrate within the peripheral region (216, for example fig. 2), wherein both the first lead lines and the first conductive layer belong to a same film layer; a plurality of second lead lines (222, for example fig. 3), disposed over the transparent substrate within the

peripheral region (216, for example fig. 3), wherein both the second lead lines and the second conductive layer belong to a same film layer.

However, Chu did not disclose a first shielding layer, disposed. over the transparent substrate within the peripheral region to cover the gaps between neighboring first lead lines, and both the first shielding layer and the second conductive layer belong to a same film layer.

Hsu discloses a first shielding layer (77, for example fig. 8), disposed over the transparent substrate (column 3, lines 1-2) within the peripheral region (see drawing below) to cover the gaps between neighboring first lead lines (67, for example fig. 8), and both the first shielding layer and the second conductive layer belong to a same film layer; Hsu also discloses a second shielding layer (left side of 56, for example fig. 2) disposed over the transparent substrate (column 3, lines 1-2) within the peripheral region (see drawing below) to cover the gaps between neighboring second lead lines (67, for example fig. 8), and both the second shielding layer and the first conductive layer belong to the same film layer; Hsu further discloses a plurality of first bonding pads (bottom reference number 55, for example fig. 2), disposed over the transparent substrate (column 3, lines 1-2) within the peripheral region (see drawing below) and connected to the first lead lines (67, for example fig. 3), wherein the first bonding pads and the first conductive layer belongs to the same film layer; a plurality of second bonding pads (left reference number 55, for example fig. 2), disposed on the transparent substrate (column 3, lines 1-2) within the peripheral region (see drawing

below) and connected to the second lead lines, wherein the second bonding pads and the second conductive layer belong to a same film layer.



With respect to claim 13, Chu discloses wherein the first conductive layer comprises a gate layer (302, for example fig. 3), and the second conductive layer comprises a source/drain layer (306, for example fig. 3).

With respect to claim 14, Chu discloses wherein the first conductive layer comprises a source/drain layer (306, for example fig. 3), and the second conductive layer comprises a gate layer (302, for example fig. 3).

Claims 10-12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chu et al. (20050062910) and Hsu as applied to claim 1, above and further in view of Sekine (6,580,486),

With respect to claim 10-12, Chu discloses invention set forth to claim 1-3, but did not disclose a common voltage is applied to the first shielding layer, second shielding layer.

Sekine discloses wherein a common voltage is applied to the first shielding layer, second shielding layer

Since Chu and Sekine are both from the same field of endeavor LCD device, the purpose disclosed by Sekine would have been recognized in the pertinent art of Chu.

Therefore, it would have been obvious to one having ordinary skill in the art at the time of the invention to have Sekine common voltage use in Chu's invention f or the purpose of reduce noise generated following voltage fluctuation between the data lines, and to improve image quality.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tsz K. Chiu whose telephone number is 517-272-8656. The examiner can normally be reached on 0800 to 1700.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Zandra V. Smith can be reached on 571-272-2429. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

TKC
March 31, 2006

Zandra V. Smith
Supervisory Patent Examiner
3 April 2006